Roll No. .....

24324

B.Tech. 6th Semester (AEIE) Examination – May, 2014

DIGITAL SYSTEM DESIGN

Paper : EE-310-F

Time : Three Hours] [M.M. : 100

Before answering the question, candidates should ensure that they have been supplied the correct and complete question paper. No complain in this regard, will be entertained after examination.

Note : Attempt ***five*** questions out of ***nine*** questions. Question No. **1** is ***compulsory*** and attempt one question from each of the ***four*** Section.

1. (a) What are the basic design units in VHDL ?

(b) Write VHDL code for 4 : 1 multiplexer using case statement.

(c) Write VHDL code for a 4 bit comparator.

(d) Compare PALs with PALs. 5 x 4

SECTION-A

2. (a) Discuss in detail about different delay models in VHDL. 14

   (b) Discuss the various operators used in VHDL. 6

3. Explain the difference between the following :

   (a) Signal and Variable

   (b) IF and Case Statement

   (c) Process and Wait statement

   (d) Arrays and Loops 5 x 4

SECTION-B

4. Explain the following :

   (a) Component declaration and component instantiation.

   (b) Generics

   (c) Procedures

   (d) Packages and Libraries 5 x 4

5. (a) Write VHDL code for design of Full adder using half adder. 10

(b) What is need of configuration in VHDL ? Explain with the help of an example. 10

SECTION-C

6. Write VHDL Codes for following :

(i) 3 bit up Counter

(ii) 1 : 16 demultiplexer

(iii) 4 bit Serial in parallel out Register

(iv) 2 : 4 decoder. 5 x 4

7. (a) Write VHDL Code for design of an MOD-10 asynchronous counter. 10

(b) Implement the Boolean function F = B + CD + AE by :

(i) NAND-NAND Logic

(ii) NOR-NOR Logic. 10

SECTION-D

8. Write short notes on : 6, 7, 7

(i) PEELs

(ii) FPGA

(iii) CPLDs

9. (a) Design a 4 bit ALU in VHDL. 10

(b) Implement $F1 = \Sigma (2, 3, 7, 9, 12, 14, 15)$

$F2 = \Sigma (2, 4, 5, 10, 11, 14, 15)$

$F3 = \Sigma (2, 3, 5, 7)$

Using 4 x 4 PAL. 10