Roll No. .....

24327

B. Tech. (ECE) 6th Sem.

Examination – May, 2015

VLSI DESIGN

Paper : EE-306-F

Time : Three Hours] *[Maximum Marks : 100*

Before answering the question, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt ***five*** questions in all, selecting ***one*** question from each Section. including Q. No. **1** which is ***compulsory.*** All questions carry equal marks.

1. (a) Discuss the small signal equivalent Ckt of a MOSFET transistor. 5

(b) What arc PMOS logic gate consideration ? 5

(c) Explain different C-MOS logic structures. 5

(d) Discuss different types of packages in VHDL. 5

SECTION – A

2. (a) Explain working of N-MOS depletion and N-MOS enhancement transistor. 10

(b) Discuss various steps involved in Bi CMOS fabrication. 10

3. (a) Discuss MOS device design equations into these region. 10

(b) Discuss various 2nd order effects MOS Transistor Model. 10

SECTION – B

4. Show that pull up to pull down ratio ie Zp.u/Zp.d for an n-MOS inverter driven by another n-MOS inverter is 4 :1. 20

5. (a) Discuss various alternative form of Pull-up. 10

(b) Discuss briefly Super buffers Bi CMOS and steering logic. 10

SECTION – C

6. Discuss about the concept of two phase clocking. Also explain problem of clock skew. 20

7. Explain the Basel stipler structure in detail also discuss two input C-MOS NAND gate. 20

SECTION – D

8. Write short notes on the following : 10 + 10 = 20

   (a) PLA and PAL

   (b) FSM

9. Discuss the different types of operators subprograms and Test benches in VHDL. 20
