22148

M.Tech. 2nd Semester (ECE) Examination, May–2017

ELECTRONICS SYSTEM DESIGN

Paper–MEEC–502

Time allowed : 3 hours] *[Maximum marks : 100*

Note : *Attempt any **five** questions.*

1. (a) Design a full subtractor using NOR gates. 10

(b) Using theorems minimize the following expression 10

$F = \overline{A}\overline{B}\overline{C}D+\overline{A}\overline{B}CD+\overline{A}BCD+\overline{A}B\overline{C}D+AB\overline{C}D+ABCD$

2. (a) Implement the following function with a multiplier with B, C and D are to be select lines :

$F(A, B, C, D) = \sum (0, 1, 3, 4, 8, 9, 15)$ 10

(b) Discuss XOR and AND-OR-Invert gates in detail. 10

3. (a) Draw the circuit diagram of R–S type flip-flop. Design a JK flip flop using R–S flip flop. 10

(b) What are basic clocking aspects with flip-flops ? What is clock skew ? Describe why clock skew create data transmission problems. 10

4. (a) Discuss the design steps for next decoders. 10

(b) Explain briefly the MDS diagram construction concepts with flow diagram. 10

5. (a) Differentiate between ROM, PLA and PAL. 10

(b) Explain the various design steps of asynchronous machine. 10

6. (a) Explain the concept of system controllers. Also discuss the controller design phase and system documention. 10

(b) Design and implement 2 bit comparator. 10

7. (a) Explain MEV approaches to asynchronous design. 10

(b) What are essential hazards ? How these hazards affect the operation of machines ? 10

8. Write short notes on (any *two*) : 20

(a) Excitation map

(b) Cycle and Races

(c) MSI Decoders.