Roll No. .....

24324

B. Tech. (AEIE) 6th Sem.

Examination – May, 2015

DIGITAL SYSTEM DESIGN

Paper : EE-310-F

Time : Three Hours] *[Maximum Marks : 100*

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt ***five*** questions out of 9 questions. Question No. 1 is ***compulsory*** and attempt ***one*** question form each of four Sections. All questions carry equal marks.

1. (a) Discuss the different classes of VHDL objects.

(b) Explain Loop statement used in VHDL with suitable example.

(c) Write VHDL code for half subtractor.

(d) Discuss in brief about GAL. $5 \times 4 = 20$

SECTION – A

2. (a) Write in detail about various data types and operators used in VHDL. 10

(b) What is overloading ? Explain overloading in VHDL with suitable example. 10

3. Write VHDL code for design of full subtractor using :

(i) behaviour style of modelling,

(ii) structural style of modelling. 10 + 10 = 20

SECTION – B

4. (a) Write VHDL code for design of S-R flip flop using ASSERT statement. 10

(b) Write in detail about packages and libraries used in VHDL. 10

5. (a) Write VHDL code for 4 : 1 multiplexer using :

(i) Case statement,

(ii) If THEN ELSE statement. 10

(b) What is difference between function and procedures ? Explain with example. 10

SECTION – C

6. (a) Write VHDL code for BCD to seven segment decoder using dataflow and structural style of modelling. 15

(b) Write VHDL code for 4 bit Serial in Serial out register. 5

7. Write VHDL code for 3 bit up counter using all the three styles of modelling. 20

SECTION – D

8. Write short notes on : 7 + 7 + 6 = 20

(i) FPGA

(ii) PAL + PLA

(iii) PEEL

9. (a) Draw and discuss in detail about architecture of simple micro computer system. 10

(b) Implement $F(A,B,C) = \Sigma(2,4,6,7)$ using PLA. 10