B.Tech. 7th Semester Computer Science Engineering–VIII Examination, December–2013

ADVANCED COMPUTER ARCHITECTURE

Paper–CSE–401-F

Time allowed : 3 hours] *[Maximum marks : 100*

*Note : Attempt **five** questions in total. **Question 1 is compulsory**. Attempt **one** question from each section.*

1. (a) Define the terms command and machine. 20

(b) Differentiate between horizontal and vertical instruction.

(c) Differentiate between warm and cold cache.

(d) What do you mean by hit ratio and miss rate ?

(e) What is a memory module ?

(f) What do you mean by closed queue ?

(g) Name various run time scheduling techniques.

(h) What do you mean by clustering ?

Section–A

2. (a) Differentiate between hardwired control and micro programmed control. 10

(b) Assume a wafer has diameter of 0.30 m and costs 1000 for a particular production run. Compute the cost per die for die area = 1.5 cm^2 and for 0.035 m^2 if defect density = 0.8 defects/cm^2. 10

3. (a) Write a program in L/S, R/M architecture for addition of a constant value in all the elements of an array. 10

(b) What is cycle quantization ? Find the effect of cycle quantization on pipelining. 10

Section–B

4. (a) Explain various cache write policies. 10

(b) We have a two level cache with miss rate of 5% (L1) and 2% (L2). Suppose the miss in L1 and hit in L2 penalty is 3 cycle and miss penalty in both caches is 6 cycles. If a processor makes 1.4 references per instruction, Compute excess CPI due to cache misses. 10

5. Write notes on :

   (a) Overlapping T cycle in virtual to real translation. 10

   (b) Explain full associative mapping scheme. 10

Section–C

6. Explain Hellerman, Strecker and Rau's model in memory system design. 20

7. Explain Flores and closed queue model. 20

Section–D

8. (a) Explain various functional units of multiple issue machine. 10

   (b) Explain snoopy and directory based protocols. 10

9. Write notes on :

   (a) Comparison of vector processor and multiple issue machines. 10

   (b) Memory coherency in shared memory multiprocessor. 10