M.Tech. 2nd Semester (ECE) CBCS Examination,

May–2017

VLSI DESIGN

Paper–MTECE22D4

Time allowed : 3 hours] *[Maximum marks : 100*

Note : ***Q. No. 1 is compulsory.*** *Attempt any* ***one*** *question from each section.*

1. Explain the following :

(a) Body Effect. 5

(b) CMOS Design Rules 5

(c) Thermal Aspect of Processing in the MOS Technology. 5

(d) Architectural issues in VLSI. 5

Section–A

2. (a) What is the meaning of depletion in MOSFET ? Discuss in brief the theory of depletion type MOSFET with suitable diagrams used. 10

(b) What is the difference between N-MOS and P-MOS ? Which one is preferred over the other ? Explain in detail. 10

3. What do you mean by fabrication process ? Explain in brief the CMOS fabrication process using Twin-Tub process in detail. 20

Section–B

4. In the inverter circuit, what is meant by $Z_{P.U.}$, and $Z_{P.d}$? Derive the required ratio between $Z_{P.U.}$, and $Z_{P.d.}$ if an n-MOS inverter is to be driven from another n-MOS inverter. 20

5. (a) What do you mean by Latch-up problem in CMOS circuit ? How can it be avoided ? Explain. 10

   (b) Explain the operation of Pass transistor ? Can it be used as an AND Gate ? Explain. 10

Section–C

6. (a) What is the meaning of Stick Diagram ? Why it is used ? What are the different rules for designing a stick diagram ? Explain. 10

   (b) What do you mean by the following :

   (i) Delay unit and inverter delay.

   (ii) Propagation Delay. 10

7. Draw stick diagram of the given equation :

   (i) Y=A+B+CD 7

   (ii) 2-input XOR Gate 7

   (iii) CMOS Buffer. 6

Section–D

8. What is the meaning of Scaling of MOS transistors ? What are the different factors used in scaling? Explain. Also discuss about the limitations of the scaling. 20

9. Explain the following :

   (i) Design of ALU Subsystem 6

   (ii) FSM 7

   (iii) PLA. 7